CLAIMS

1. A method of manufacturing a trench gate semiconductor device comprising the steps of:

providing a silicon device body (1) having a first major surface (22), the silicon device body having a drain region (2, 4) of a first conductivity type and a body region (6) over the drain region;

forming a trench (8) extending downwards into the silicon device body from the first major surface (22), the trench having sidewalls (28) and a base (29);

etching the silicon at the base of the trench to form porous silicon (26) at the base of the trench; and

thermally oxidising the device to oxidise the porous silicon at the bottom of the trench to form a plug (30) at the base of the trench; and

depositing conductive material within the trench (8) to form a gate (34).

2. A method according to claim 1 further comprising, after the step of etching the trench, the step of lining the side walls (28) of the trench with dielectric liner (50) for preventing the side walls becoming porous during the step of forming porous silicon at the bottom of the trench.

3. A method according to claim 1 wherein the step of oxidising the device forms sidewall oxide (32) on the sidewalls (28) of the trench, the method further comprising the steps of etching away the oxide formed on the side wall oxide and of forming the gate oxide by thermal oxidation on the side wall before the step of depositing conductive material within the trench to form a gate.

4. A method according to any preceding claim wherein the step of forming the trench includes providing a mask (22) on the first major surface defining an opening (24) and etching the trench (8) extending downwards from the first major surface through the opening.

5. A method according to claim 4 wherein the mask (22) is an oxide hard mask.

6. A method according to claim 4 or 5 wherein the step of etching the silicon at the bottom of the trench to form porous silicon includes dry-etching the bottom of the trench through the same mask (22) used to define the trench.

7. A method according to any preceding claim further comprising depositing a silicon plug in the trench wherein the step of etching the silicon at the bottom of the trench includes etching the silicon plug.

8. A method according to any preceding claim further comprising forming a source implant (14) of first conductivity type at the first major surface adjacent to the trench and forming source (36), gate (38) and drain (40) electrodes attached to the source implant (14), the gate (34) and the drain region at the bottom of the trench respectively to complete the trench gate semiconductor device.

9. A trench MOSFET comprising:

a drain region (2, 4) of first conductivity type;

a body region (6) over the drain region;

a trench (8) extending from a first major surface (22) through the body region (6);

source regions (14) of the first conductivity type laterally adjacent to the trench (8) at the first major surface (22);

thermal gate oxide (12) on the side walls of the trench;

a gate electrode (34) in the trench insulated from the body region by the gate oxide;

characterised by a thick oxide plug (30) formed of oxidised porous silicon at the base (29) of the trench (8) extending into the drain region (2, 4).

10. A trench MOSFET according to claim 9 wherein the body region (6) is of second conductivity type opposite to the first conductivity type.